PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Nishant Sinha	**Examiner:**	Unknown
Serial No.:	Not Yet Assigned	**Group Art Unit:**	Unknown
Filed:		**Attorney Docket No.:**	2269-5859US (02-0390.00/US)
Title:	PROCESS AND INTEGRATION SCHEME FOR FABRICATING CONDUCTIVE COMPONENTS, THROUGH-VIAS AND SEMICONDUCTOR COMPONENTS INCLUDING CONDUCTIVE THROUGH-WAFER VIAS		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE UNDER 37 CFR § 3.73(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

MICRON TECHNOLOGY, INC., assignee of the entire right, title and interest by assignment from the inventor(s) in the above-identified application, hereby appoints the following attorneys and agents:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Laurence B. Bond, Reg. No. 30,549
Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393	H. Dickson Burton, Reg. No. 48,396
Allen C. Turner, Reg. No. 33,041	Edgar R. Cataxinos, Reg. No. 39,931	Kent S. Burningham, Reg. No. 30,453
Brick G. Power, Reg. No. 38,581	Kevin K. Johanson, Reg. No. 38,506	Krista Weber Powell, Reg. No. 47,867
Shawn G. Hansen, Reg. No. 42,627	Bretton L. Crockett, Reg. No. 44,632	Tawni L. Wilhelm, Reg. No. 47,456
Bradley B. Jensen, Reg. No. 46,801	Andrew F. Nilles, Reg. No. 47,825	Greg T. Warder, Reg. No. 50,208
Katherine A. Hamer, Reg. No. 47,628	Marcus S. Simon, Reg. No. 50,258	Trent N. Butcher, Reg. No. 51,518
G. Scott Dorland, Ph.D., Reg. No. 51,622	Michael L. Lynch, Reg. No. 30,871	Charles B. Brantley II, Reg. No. 38,086

as its attorneys with full power of substitution to prosecute this application and all applications claiming filing date priority therefrom and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

The above-identified assignee hereby elects, pursuant to 37 C.F.R. § 3.71, to conduct the prosecution of the above-identified patent application to the exclusion of the inventor(s).

A chain of title from the inventor(s) of the above-identified patent application to the above-identified assignee is shown:

☐ In an assignment recorded in the U.S. Patent and Trademark Office at Reel _____, Frame _____.

☒ In an assignment filed herewith for recordation, a true copy of which is attached hereto.

The undersigned has reviewed the above-identified assignment and, to the best of his knowledge and belief, title is in the above-identified assignee.

The undersigned further avers that he is empowered to make and sign the foregoing certification on behalf of the above-identified assignee, and to take the action set forth herein on its behalf.

Please direct all communications regarding the above-identified application to:

Joseph A. Walkowski,
TRASKBRITT
P.O. Box 2550
Salt Lake City, UT 84110
Telephone: (801) 532-1922
Fax: (801) 531-9168

Respectfully submitted,

MICRON TECHNOLOGY, INC.

Date: 9-17-2003

By: _____
Michael L. Lynch, Esq.
Reg. No. 30,871
Chief Patent Counsel,
MICRON TECHNOLOGY, INC.

Document in ProLaw

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled PROCESS AND INTEGRATION SCHEME FOR FABRICATING CONDUCTIVE COMPONENTS, THROUGH-VIAS AND SEMICONDUCTOR COMPONENTS INCLUDING CONDUCTIVE THROUGH-WAFER VIAS, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority	Claimed
_____	_____	_____	_____	_____
(number)	(country)	(day/month/year filed)	Yes	No
_____	_____	_____	_____	_____
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to

DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention Title: PROCESS AND INTEGRATION SCHEME FOR FABRICATING CONDUCTIVE COMPONENTS, THROUGH-VIAS AND SEMICONDUCTOR COMPONENTS INCLUDING CONDUCTIVE THROUGH-WAFER VIAS

patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status–pending, patented or abandoned)
(application serial no.)	(filing date)	(status–pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David V. Trask, Reg. No. 22,012
Laurence B. Bond, Reg. No. 30,549
James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041
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Salt Lake City, Utah 84110

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(continuation page)

Invention Title: PROCESS AND INTEGRATION SCHEME FOR FABRICATING CONDUCTIVE COMPONENTS, THROUGH-VIAS AND SEMICONDUCTOR COMPONENTS INCLUDING CONDUCTIVE THROUGH-WAFER VIAS

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first joint inventor: Nishant Sinha

Inventor's signature _____ Date 9/19/03
Residence: Boise, ID
Citizenship: India
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